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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,776	02/25/2002	Victor A. Bennett	BENNETT 6-5	4410

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,776	BENNETT ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2002 and 12 September 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-42 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Drawings as filed on 12 September 2002

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Figure 3, element 324. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 2, 9, and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Examiner could not determine where in the specification an apparatus and/or method for *preventing* a thread from executing until a device request is fulfilled (Applicant's claim 1) and for *allowing* said thread to continue to traverse the pipeline while waiting for said device request to be fulfilled (Applicant's claim 2). When an instruction traverses a pipeline, it is being executed.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 2, 9, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear how an apparatus and/or method for *preventing* a thread from executing until a device request is fulfilled (Applicant's claim 1) can also *allow* said thread to continue to traverse the pipeline while waiting for said device request to be fulfilled (Applicant's claim 2). When an instruction traverses a pipeline, it is being executed.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-3, 6-10, 13-14 are rejected under 35 U.S.C. 102(b) as being taught by Parady, U.S. Patent Number 5,933,627 (herein referred to as Parady).

11. Referring to claim 1, Parady has taught a context switching system for a multi-thread execution pipeline loop having a pipeline latency, comprising:

a. A context switch requesting subsystem configured to:

i. Detect a device request from thread executing within said multi-thread execution pipeline loop for access to a device having a fulfillment latency exceeding said pipeline latency (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3), and

ii. Generate a context Switch request for said thread (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3); and

b. A context controller subsystem configured to receive said context switch request and prevent said thread from executing until said device request is fulfilled (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3).

12. Referring to claim 8, Parady has taught for use with a multi-thread execution pipeline loop having a pipeline latency, a method of operating a context switching system, comprising:

a. Detecting a device request from a thread executing within said multi-thread execution pipeline loop for access to a device having a fulfillment latency exceeding said pipeline latency (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3);

b. Generating a context switch request for said thread when said thread issues said device request (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3); and

c. Receiving said context switch request and preventing said thread from executing until said device request is fulfilled (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3).

13. Referring to claims 2 and 9, Parady has taught wherein said context controller subsystem is further configured to allow said thread continue traverse said multi-thread execution pipeline loop while waiting for said device request to be fulfilled (Parady column 4, lines 53-62).

14. Referring to claims 3 and 10, Parady has taught wherein said context controller subsystem is further configured to allow other threads within said multi-thread execution pipeline loop to continue to execute while said thread is waiting for said device request to be fulfilled (Parady column 2, lines 28-34; column 3, line 57 to column 4, line 18; column 4, line 42-62; and Figure 3).

15. Referring to claims 6 and 13, Parady has taught wherein said context controller subsystem *is* further configured to replace said thread's current instruction with a NO-Operation (NOP) instruction to prevent said thread from executing until said device request is fulfilled (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3). In regards to Parady, when a context switches occurs between a current thread and the next thread, the current thread becomes, in essence NOPs, since the instructions from the current thread are no longer actively being executed. The current threads instructions do nothing, which is the definition of a NOP. Please see Rosenberg's Computers, Information Processing & Telecommunications Second Edition ©1987 for clarification of the definition of NOP.

16. Referring to claims 7 and 14, Parady has taught wherein said device request is a request to access external memory due to a cache miss status (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 4-5 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent Number 5,933,627 (herein referred to as Parady), as applied to claims 1 and 8 above, in view of Kon and Medina's Round-Robin Scheduling © 29 January 1996 (herein

referred to as Kon). Parady has not explicitly taught a miss fulfillment first-in-first-out buffer (FIFO), said context controller subsystem further configured to employ said FIFO to:

a. Store said thread in said miss fulfillment FIFO upon reaching an end position of said multi-thread execution pipeline loop (Applicant's claims 4 and 11),

b. Sequence said thread through said miss fulfillment FIFO (Applicant's claims 4 and 11), and

c. Reinsert said thread into said multi-thread execution pipeline loop at a beginning position (Applicant's claims 4 and 11).

d. Wherein said context controller subsystem is further configured to store said thread in said miss fulfillment FIFO upon receiving said context switch request (Applicant's claims 5 and 12).

19. However, Parady has taught round robin scheduling is used in the switch device (Parady column 4, lines 42-46). Kon has taught a miss fulfillment first-in-first-out buffer (FIFO), said context controller subsystem further configured to employ said FIFO to:

a. Store said thread in said miss fulfillment FIFO upon reaching an end position of said multi-thread execution pipeline loop (Applicant's claims 4 and 11) (Kon "What is Round-Robin Scheduling?"),

b. Sequence said thread through said miss fulfillment FIFO (Applicant's claims 4 and 11) (Kon "What is Round-Robin Scheduling?"), and

c. Reinsert said thread into said multi-thread execution pipeline loop at a beginning position (Applicant's claims 4 and 11) (Kon "What is Round-Robin Scheduling?").

d. Wherein said context controller subsystem is further configured to store said thread in said miss fulfillment FIFO upon receiving said context switch request (Applicant's claims 5 and 12) (Kon "What is Round-Robin Scheduling?").

20. In regards to Kon, the queue is like the FIFO buffer, since it runs the oldest, i.e. the process first put in the queue, first. Round robin scheduling is simple and effective at ensuring all threads are executed, so no thread is ever "starved." A starved thread is one that never executes, so its processes are never executed and/or completed. Round robin executes each thread for a certain interval or until a switch event, such as a long latency event, occurs, and then starts the next thread in the round robin buffer. It always executes the oldest thread in the queue first, which means that the first thread in the queue is the first thread outputted from the queue. A person of ordinary skill in the art at the time the invention was made, and as shown in Kon, would have recognized that round robin scheduling is the simplest and fairest of scheduling algorithms (Kon "What is Round-Robin Scheduling?"). Therefore, a person of ordinary skill in the art at the time the invention was made would have incorporated Kon in the device of Parady to increase simplicity and ensure fairness between threads.

21. Claims 15-17 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent Number 5,933,627 (herein referred to as Parady) in view of Wilford et al., U.S. Patent Number 5,509,006 (herein referred to as Wilford).

22. Referring to claim 15, Parady has taught a fast pattern processor that receives and processes protocol data units (PDUs), comprising:

a. A dynamic random access memory (DRAM) that contains instructions (Parady column 5, lines 19-22; Figure 5; and Figure 6). In regards to Parady, DRAM in a

specific type of RAM and Parady shows that RAM is used in his system. Please see Rosenberg's Computers, Information Processing & Telecommunications Second Edition for more information of RAM and DRAM.

b. A memory cache that caches certain of said instructions from said DRAM (Parady column 5, lines 19-22; Figure 5; and Figure 6); and

c. An engine that employs said DRAM and said memory cache to obtain ones of said instructions (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3), including:

i. A multi-thread execution pipeline loop having a pipeline latency (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3), and

ii. A context switching system for said multi-thread execution pipeline loop (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3), having:

(1) A context switch requesting subsystem that: detects a device request from a thread executing within said multi-thread execution pipeline loop for access to a device having a fulfillment latency exceeding said pipeline latency (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3), and

(2) Generates a context switch request for said thread (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3), and

iii. A context controller subsystem that receives said context switch request and prevents said thread from executing until said device request is fulfilled (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3).

23. Parady has not taught a tree engine that parses data within said PUDs. Wilford has taught a tree engine that parses data within said PUDs (Wilford column 1, lines 34-42; column 1, line 65 to column 2, line 19; column 14, lines 14-35; and Figure 5B). A person of ordinary skill in the art at the time the invention was made, and as taught in Wilford, would have recognized that a tree engine that parses data within said PUDs identifies which protocol the data belongs to in order to send the data to the correct destination (Wilford column 1, lines 34-42), thereby ensuring correct data execution. Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the tree engine of Wilford in the device of Parady to ensure correct data execution.

24. Referring to claim 16, Parady has taught wherein said context controller subsystem is further configured to allow said thread continue traverse said multi-thread execution pipeline loop while waiting for said device request to be fulfilled (Parady column 4, lines 53-62).

25. Referring to claim 17, Parady has taught wherein said context controller subsystem is further configured to allow other threads within said multi-thread execution pipeline loop to continue to execute while said thread is waiting for said device request to be fulfilled (Parady column 2, lines 28-34; column 3, line 57 to column 4, line 18; column 4, line 42-62; and Figure 3).

26. Referring to claim 20, Parady has taught wherein said context controller subsystem *is* further configured to replace said thread's current instruction with a NO-Operation (NOP) instruction to prevent said thread from executing until said device request is fulfilled (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3). In regards to Parady, when a context switches occurs between a current thread and the next thread, the current thread becomes, in essence NOPs, since the instructions from the current thread are no longer actively being executed. The current threads instructions do nothing, which is the definition of a NOP. Please see Rosenberg's Computers, Information Processing & Telecommunications Second Edition ©1987 for clarification of the definition of NOP.

27. Referring to claim 21, Parady has taught wherein said device request is a request to access external memory due to a cache miss status (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3).

28. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent Number 5,933,627 (herein referred to as Parady) in view of Wilford et al., U.S. Patent Number 5,509,006 (herein referred to as Wilford), as applied to claim 15 above, in further

view of Kon and Medina's Round-Robin Scheduling © 29 January 1996 (herein referred to as Kon). Parady has not explicitly taught a miss fulfillment first-in-first-out buffer (FIFO), said context controller subsystem further configured to employ said FIFO to:

a. Store said thread in said miss fulfillment FIFO upon reaching an end position of said multi-thread execution pipeline loop (Applicant's claim 18),

b. Sequence said thread through said miss fulfillment FIFO (Applicant's claim 18), and

c. Reinsert said thread into said multi-thread execution pipeline loop at a beginning position (Applicant's claim 18).

d. Wherein said context controller subsystem is further configured to store said thread in said miss fulfillment FIFO upon receiving said context switch request (Applicant's claim 19).

29. However, Parady has taught round robin scheduling is used in the switch device (Parady column 4, lines 42-46). Kon has taught a miss fulfillment first-in-first-out buffer (FIFO), said context controller subsystem further configured to employ said FIFO to:

a. Store said thread in said miss fulfillment FIFO upon reaching an end position of said multi-thread execution pipeline loop (Applicant's claim 18) (Kon "What is Round-Robin Scheduling?"),

b. Sequence said thread through said miss fulfillment FIFO (Applicant's claim 18) (Kon "What is Round-Robin Scheduling?"), and

c. Reinsert said thread into said multi-thread execution pipeline loop at a beginning position (Applicant's claim 18) (Kon "What is Round-Robin Scheduling?").

d. Wherein said context controller subsystem is further configured to store said thread in said miss fulfillment FIFO upon receiving said context switch request (Applicant's claim 19) (Kon "What is Round-Robin Scheduling?").

30. In regards to Kon, the queue is like the FIFO buffer, since it runs the oldest, i.e. the process first put in the queue, first. Round robin scheduling is simple and effective at ensuring all threads are executed, so no thread is ever "starved." A starved thread is one that never executes, so its processes are never executed and/or completed. Round robin executes each thread for a certain interval or until a switch event, such as a long latency event, occurs, and then starts the next thread in the round robin buffer. It always executes the oldest thread in the queue first, which means that the first thread in the queue is the first thread outputted from the queue. A person of ordinary skill in the art at the time the invention was made, and as shown in Kon, would have recognized that round robin scheduling is the simplest and fairest of scheduling algorithms (Kon "What is Round-Robin Scheduling?"). Therefore, a person of ordinary skill in the art at the time the invention was made would have incorporated Kon in the device of Parady to increase simplicity and ensure fairness between threads.

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Gregory T. Byrd and Mark A. Holliday's "Multithreaded Processor Architectures" in IEEE Spectrum ©August 1995 has described a multithreaded system.

b. Gottlieb et al., U.S. Patent Number 6,016,542, has taught thread switching on long latency instructions.

c. Hwang, U.S. Patent Number 6,216,220, has taught thread switching on long latency instructions.

d. Parady, U.S. Patent Numbers 6,295,600 and 6,578,137, has taught thread switching on long latency instructions.

e. Kalafatis et al., U.S. Patent Number 6,535,905, has taught thread switching on long latency instructions.

f. Aglietti et al., U.S. Patent Number 6,578,065, has taught thread switching on long latency instructions.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm. Gottlieb et al., U.S. Patent Number 6,016,542, has taught thread switching on long latency instructions.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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29 October 2004

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